

FIG. 1

TrCH NUMBER	RM i	THE NUMBER OF BITS PER FRAME BEFORE RATE MATCHING
TrCH#1	256	270
TrCH#2	250	690
TrCH#3	240	540
TrCH#4	200	600

FIG. 2

TrCH NUMBER	ΔN_{ij}
TrCH#1	+67(Repetition)
TrCH#2	+153(Repetition)
TrCH#3	+93(Repetition)
TrCH#4	- 13(Puncture)

FIG. 3

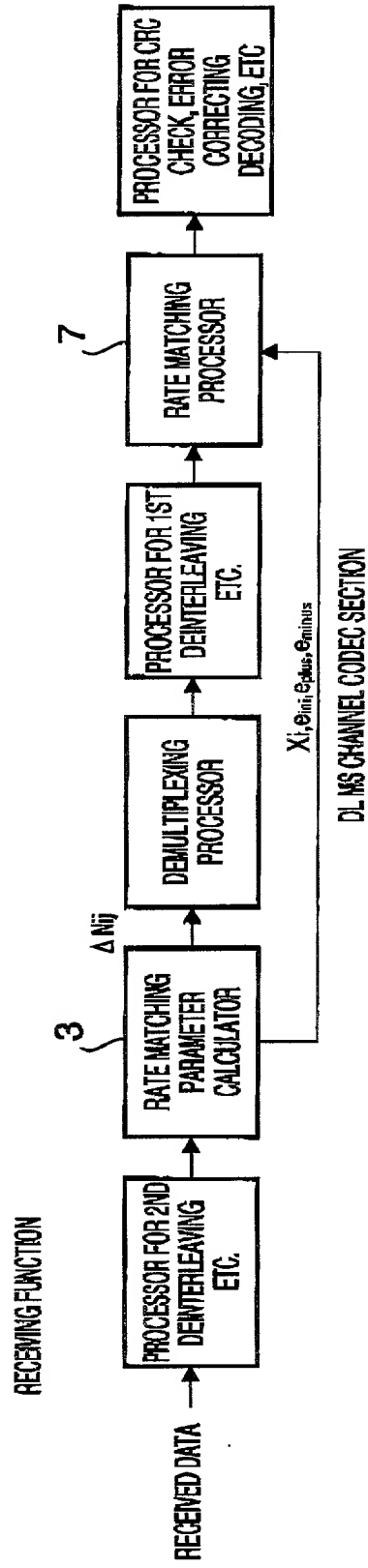


FIG. 4

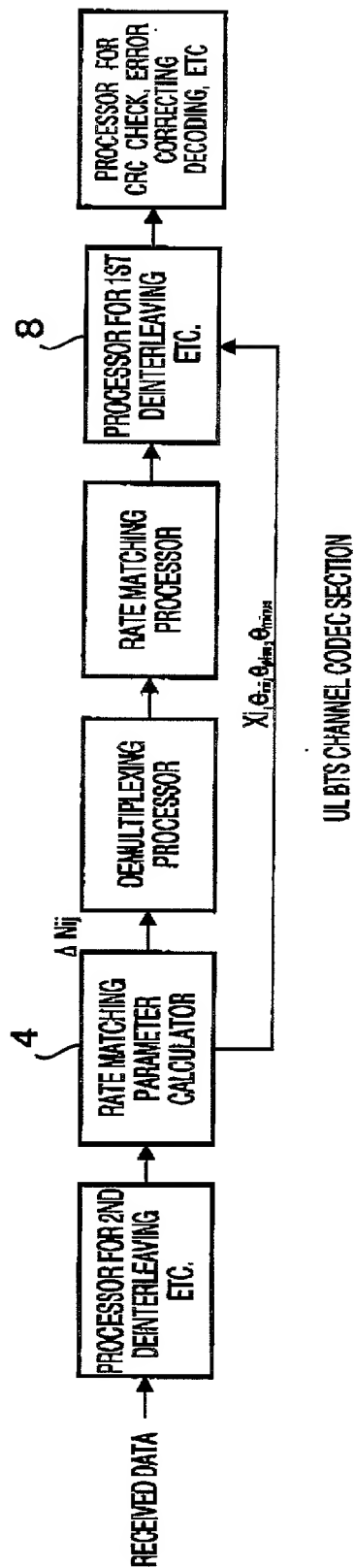


FIG. 5

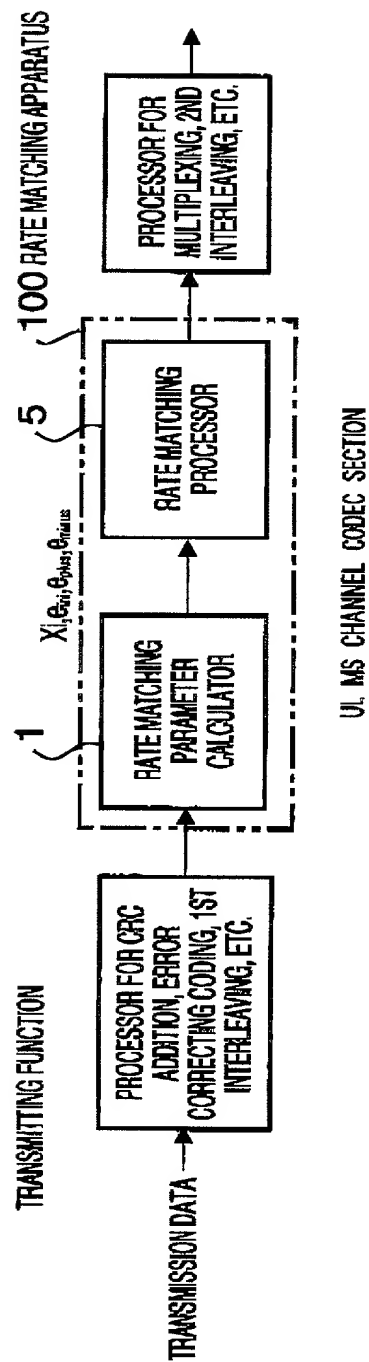
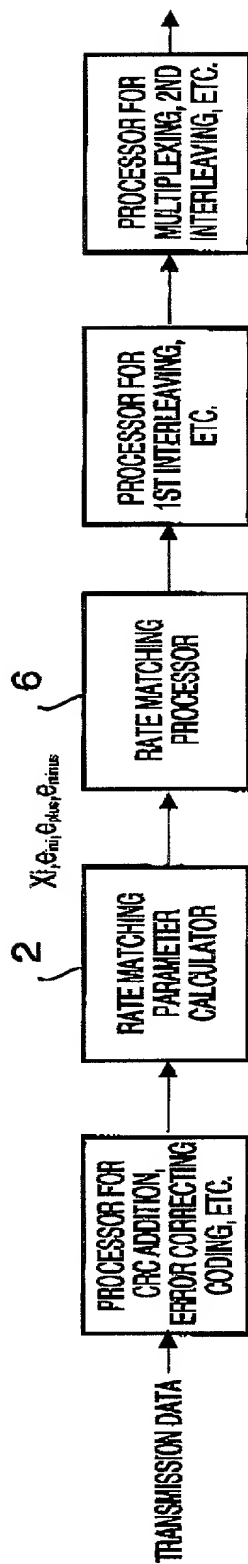


FIG. 6

FIG. 7 is a block diagram of the DL BTS channel code section. The diagram shows a sequence of processing blocks: a processor for CRC addition, error correcting coding, etc.; a rate matching parameter calculator; a rate matching processor; and a processor for 1st interleaving, etc. The final output is a processor for multiplexing, 2nd interleaving, etc. The rate matching parameter calculator and rate matching processor are grouped by a bracket labeled '2'. The rate matching processor and the final processor are grouped by a bracket labeled '6'. The input to the first processor is 'TRANSMISSION DATA'.



DL BTS CHANNEL CODEC SECTION

FIG. 7

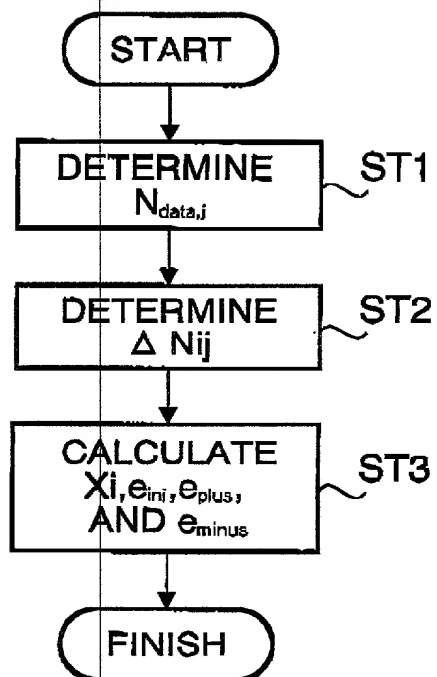


FIG. 8

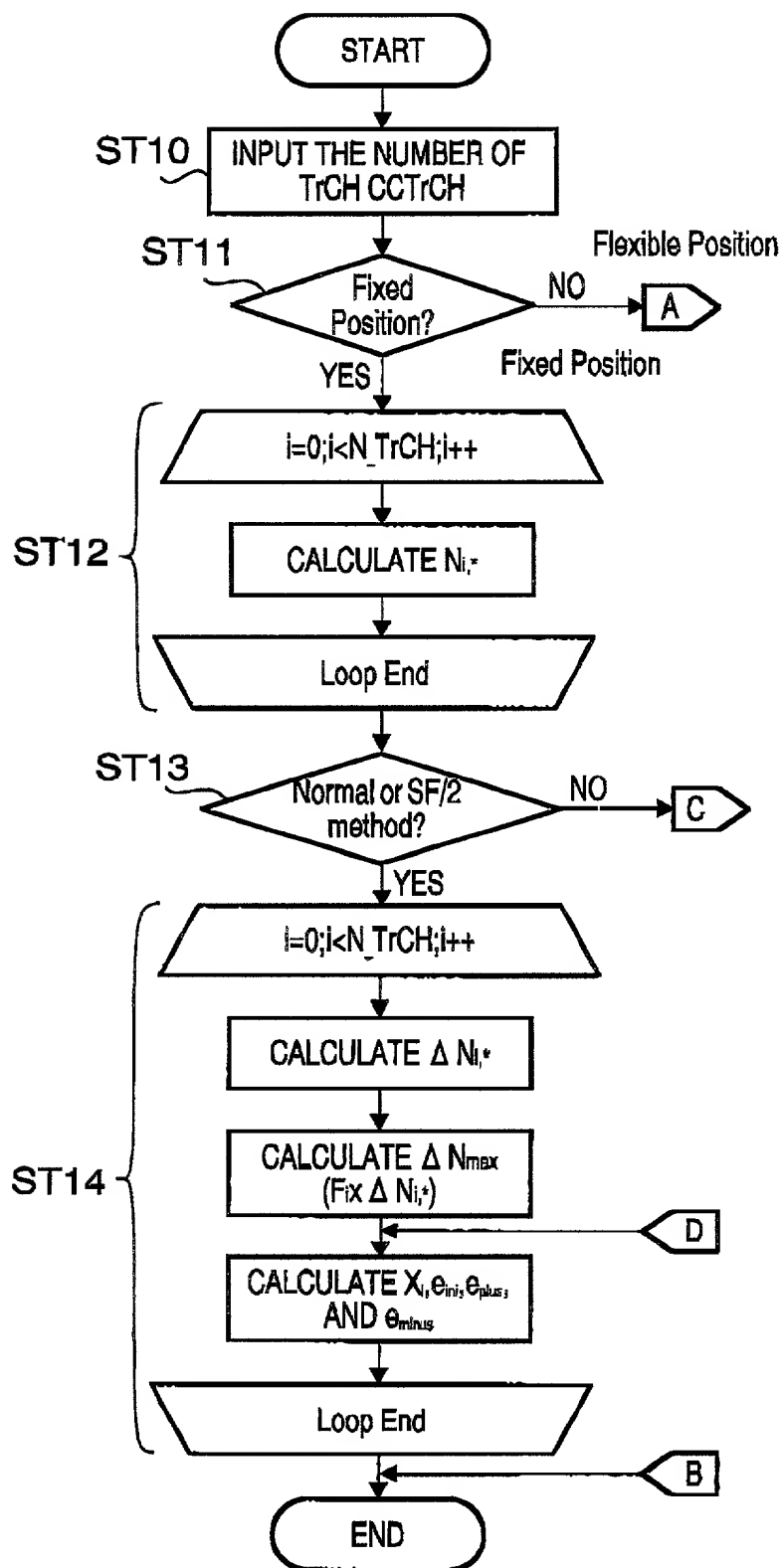


FIG. 9

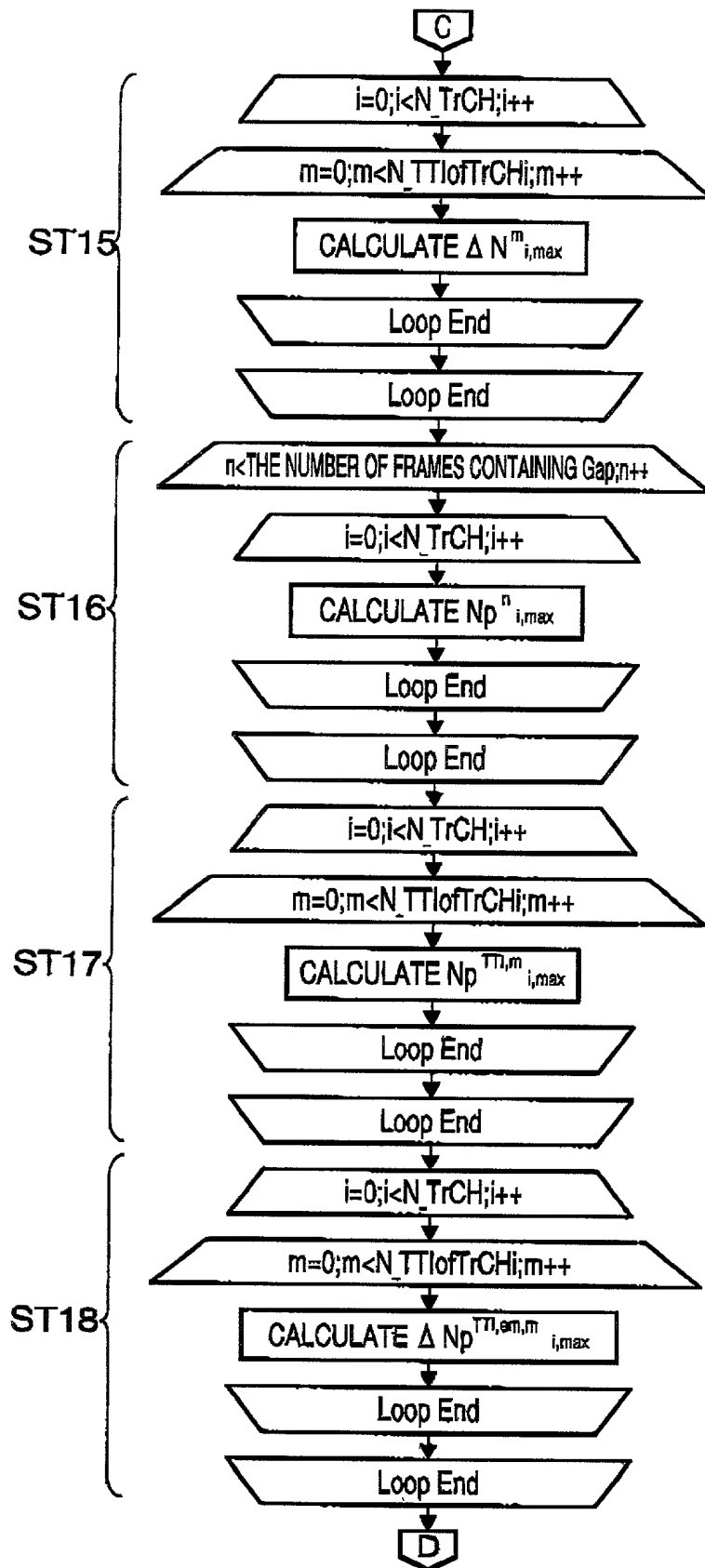


FIG. 10

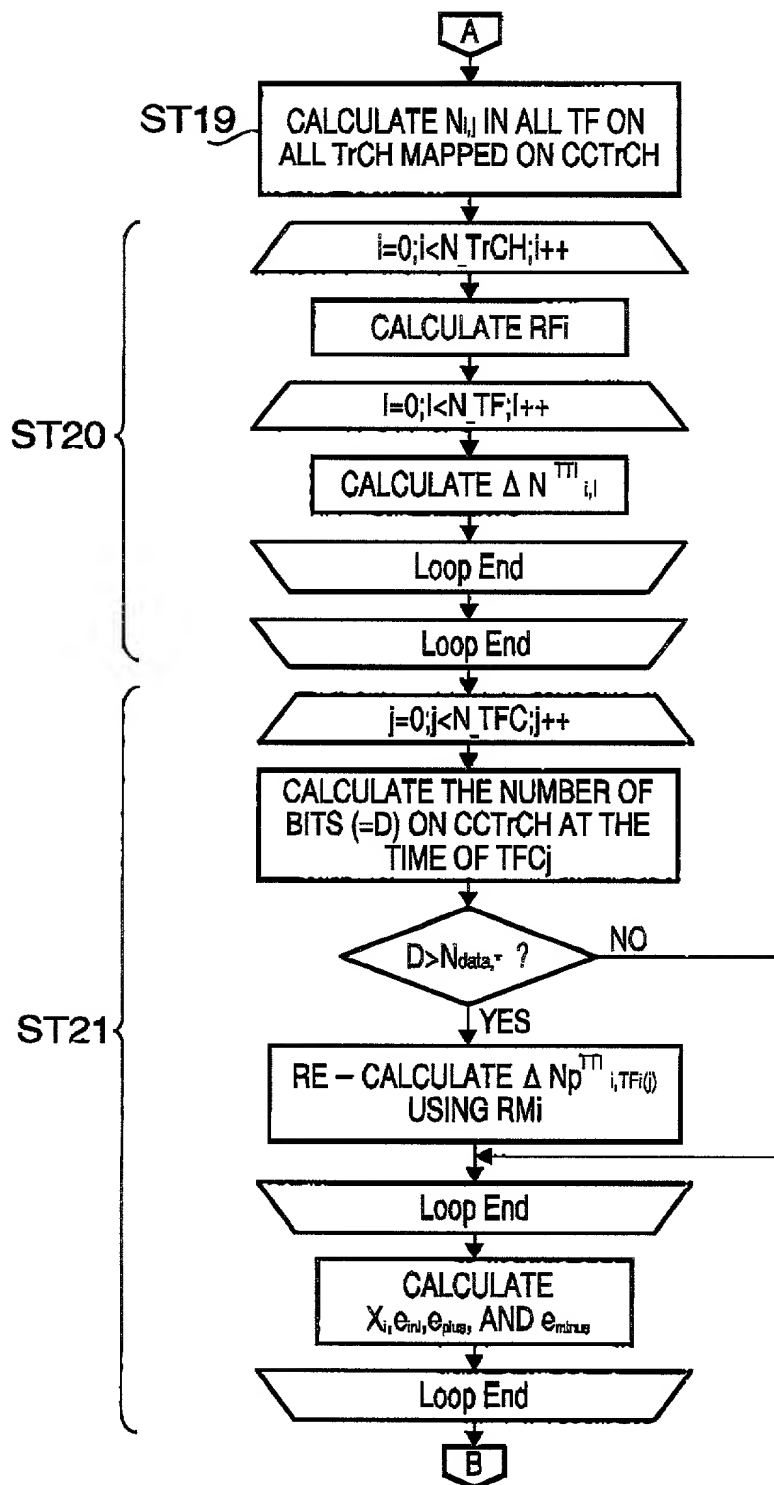


FIG.11

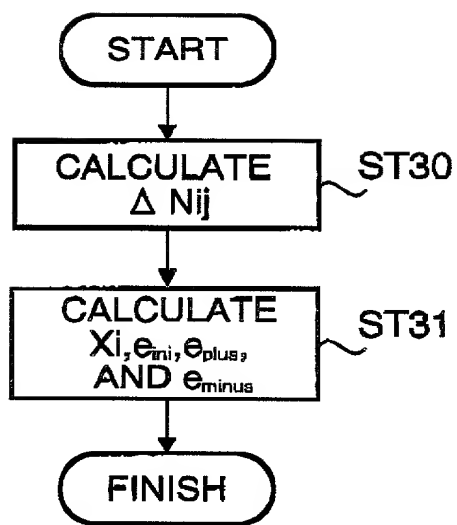


FIG.12

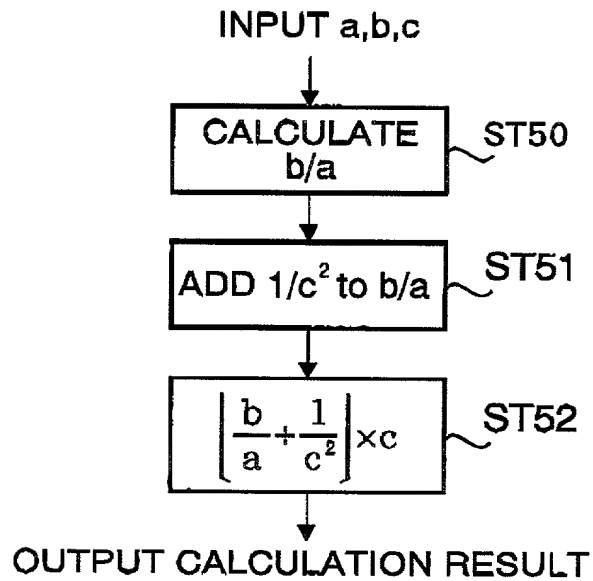


FIG.13

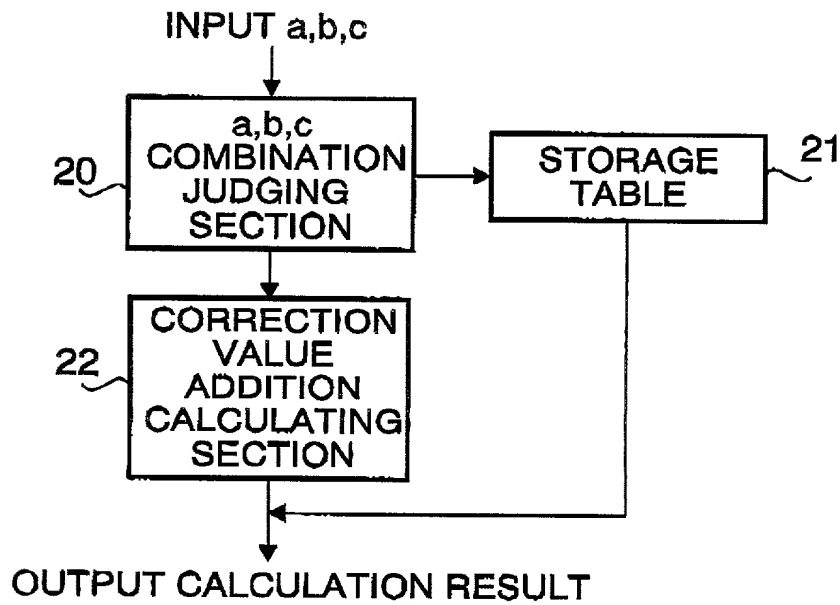


FIG.14

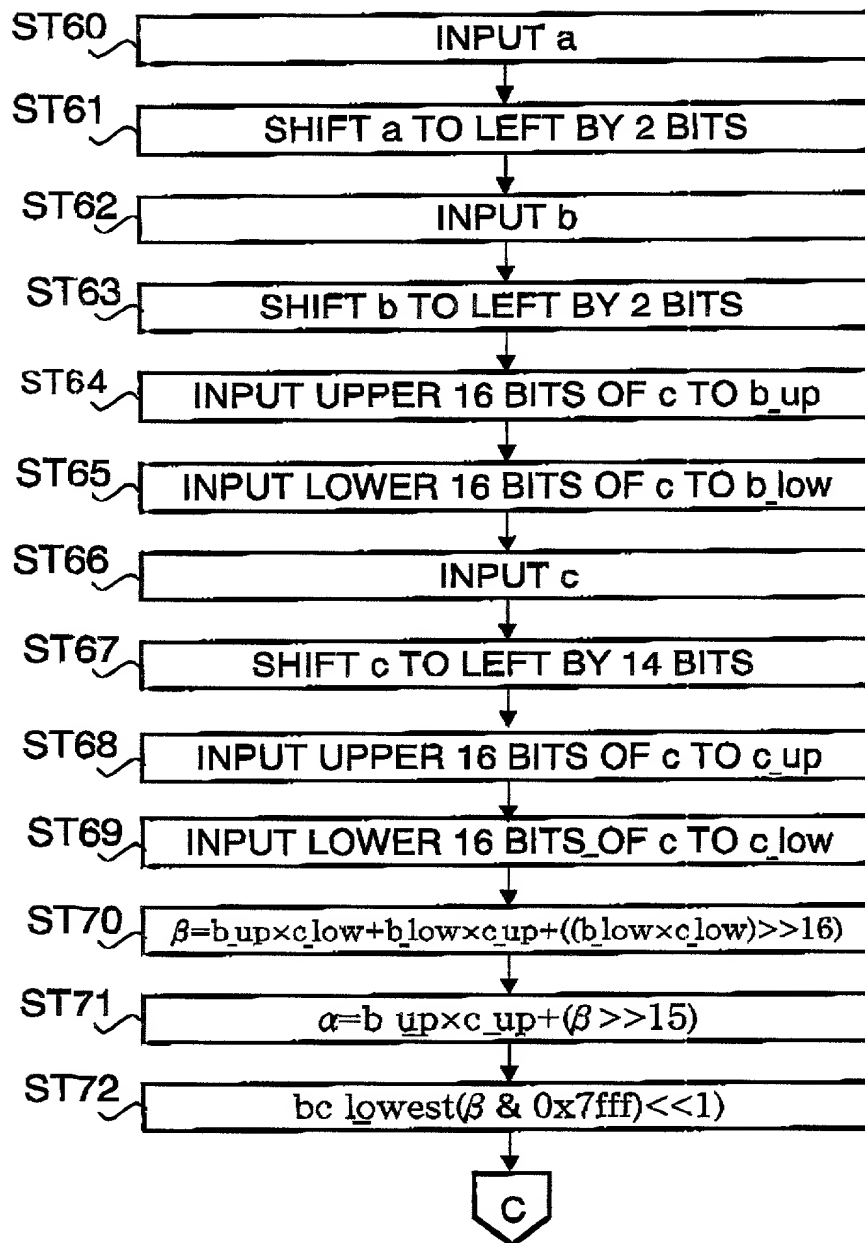


FIG.15

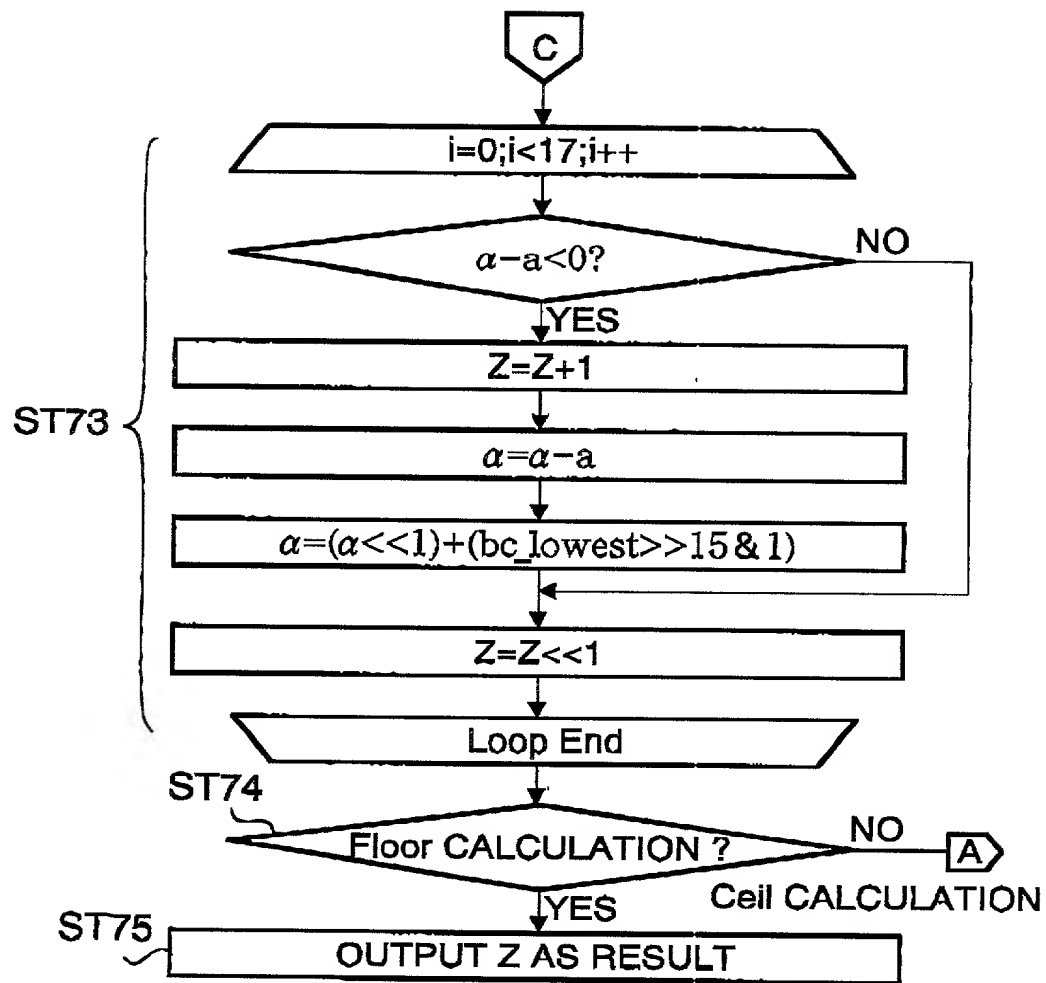


FIG. 16

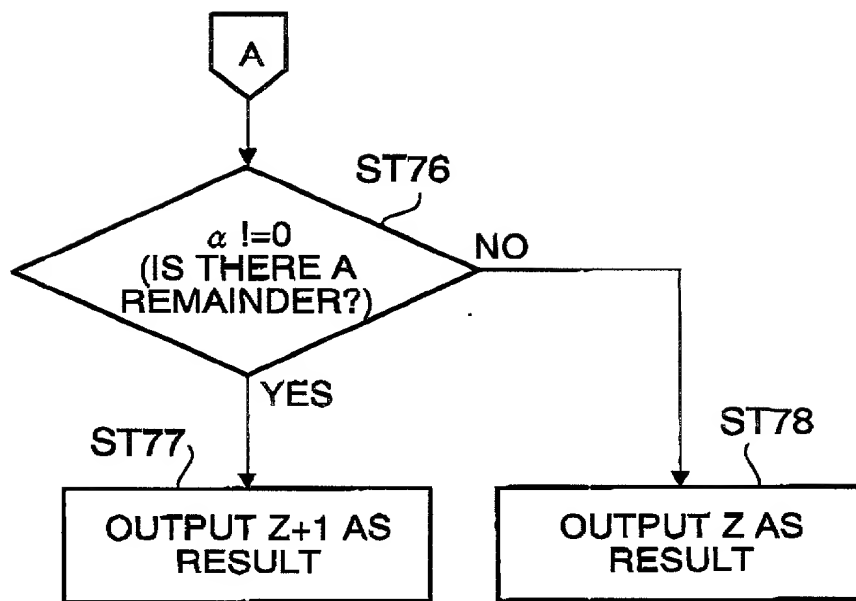


FIG.17

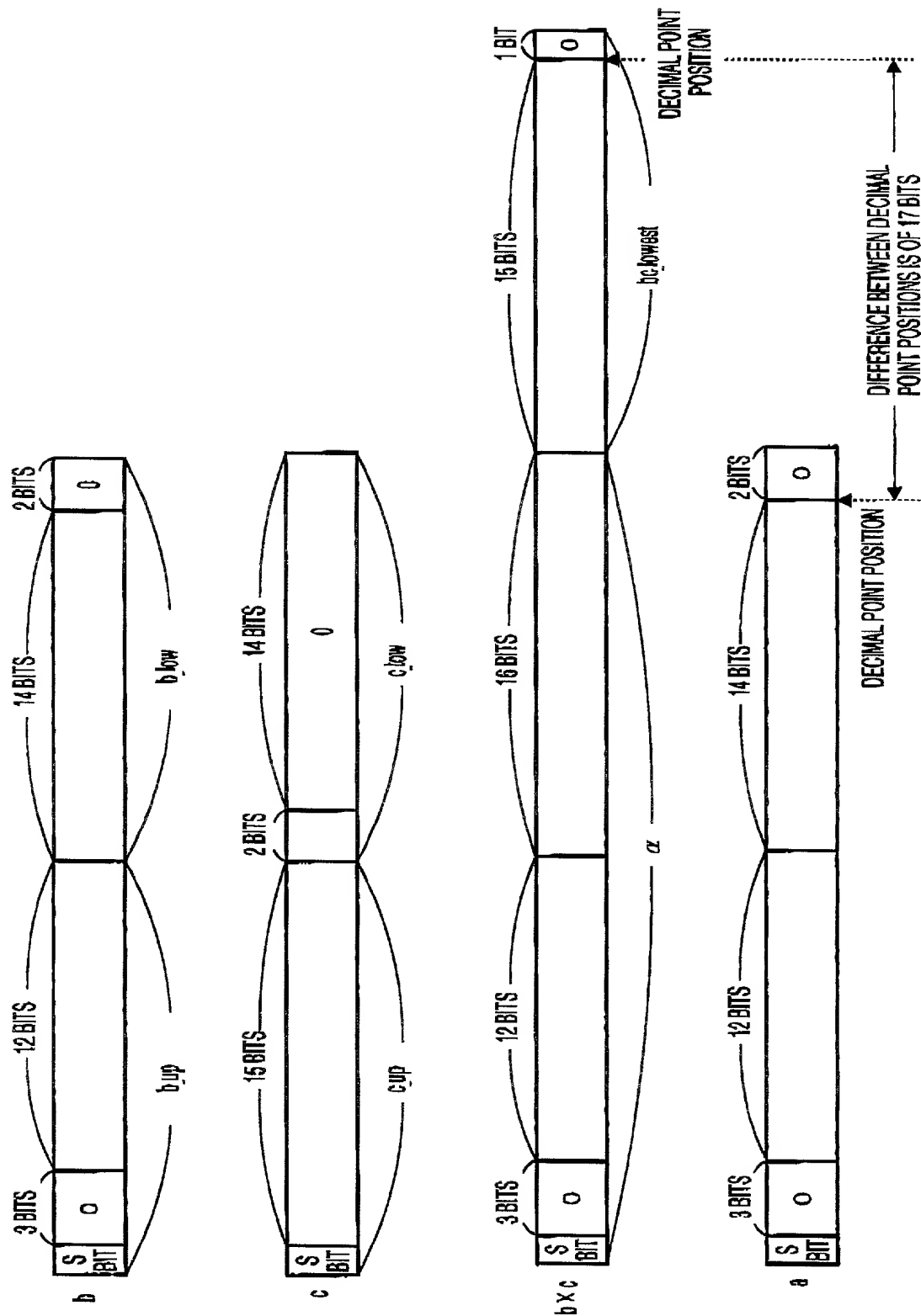


FIG.18